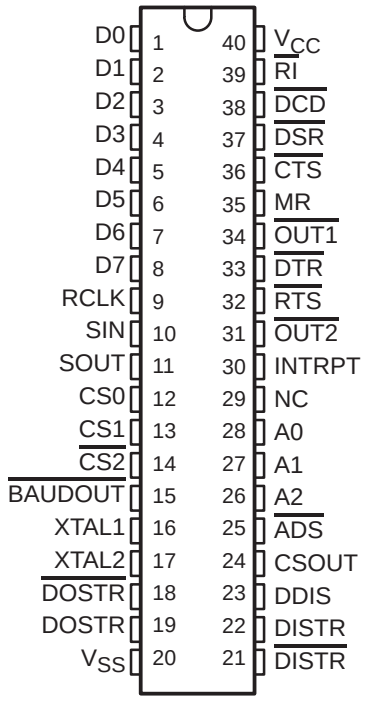
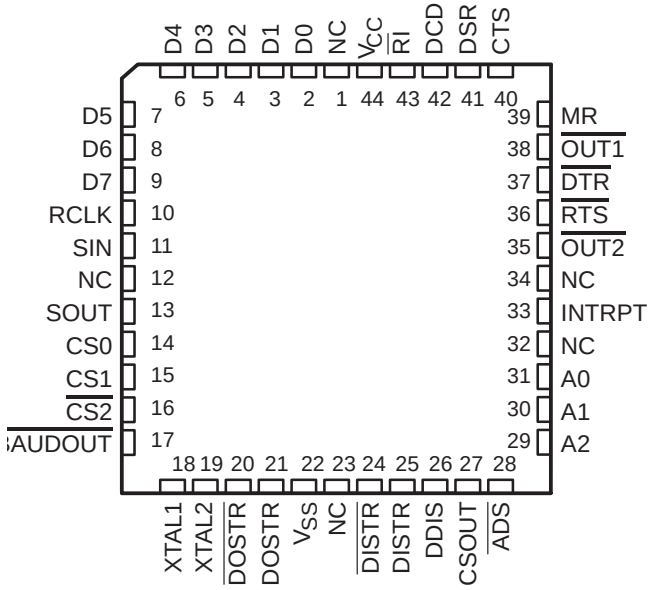
SLLS037B – MARCH 1988 – REVISED MARCH 1996

- **Programmable Baud Rate Generator Allows Division of Any Input Reference Clock by 1 to (2^{16} – 1) and Generates an Internal 16× Clock**
- **Full Double Buffering Eliminates the Need for Precise Synchronization**
- **Standard Asynchronous Communication Bits (Start, Stop, and Parity) Added or Deleted to or From the Serial Data Stream**
- **Independent Receiver Clock Input**
- **Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Generation (dc to 256 Kbit/s)**
- **False Start Bit Detection**
- **Complete Status Reporting Capabilities**
- **3-State TTL Drive Capabilities for Bidirectional Data Bus and Control Bus**
- **Line Break Generation and Detection**
- **Internal Diagnostic Capabilities:**
  - **Loopback Controls for Communications Link Fault Isolation**
  - **Break, Parity, Overrun, Framing Error Simulation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, and $\overline{DCD}$)**
- **Easily Interfaces to Most Popular Microprocessors**
- **Faster Plug-In Replacement for National Semiconductor NS16C450**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL16C450 is a CMOS version of an asynchronous communications element (ACE). It typically functions in a microcomputer system as a serial input/output interface.

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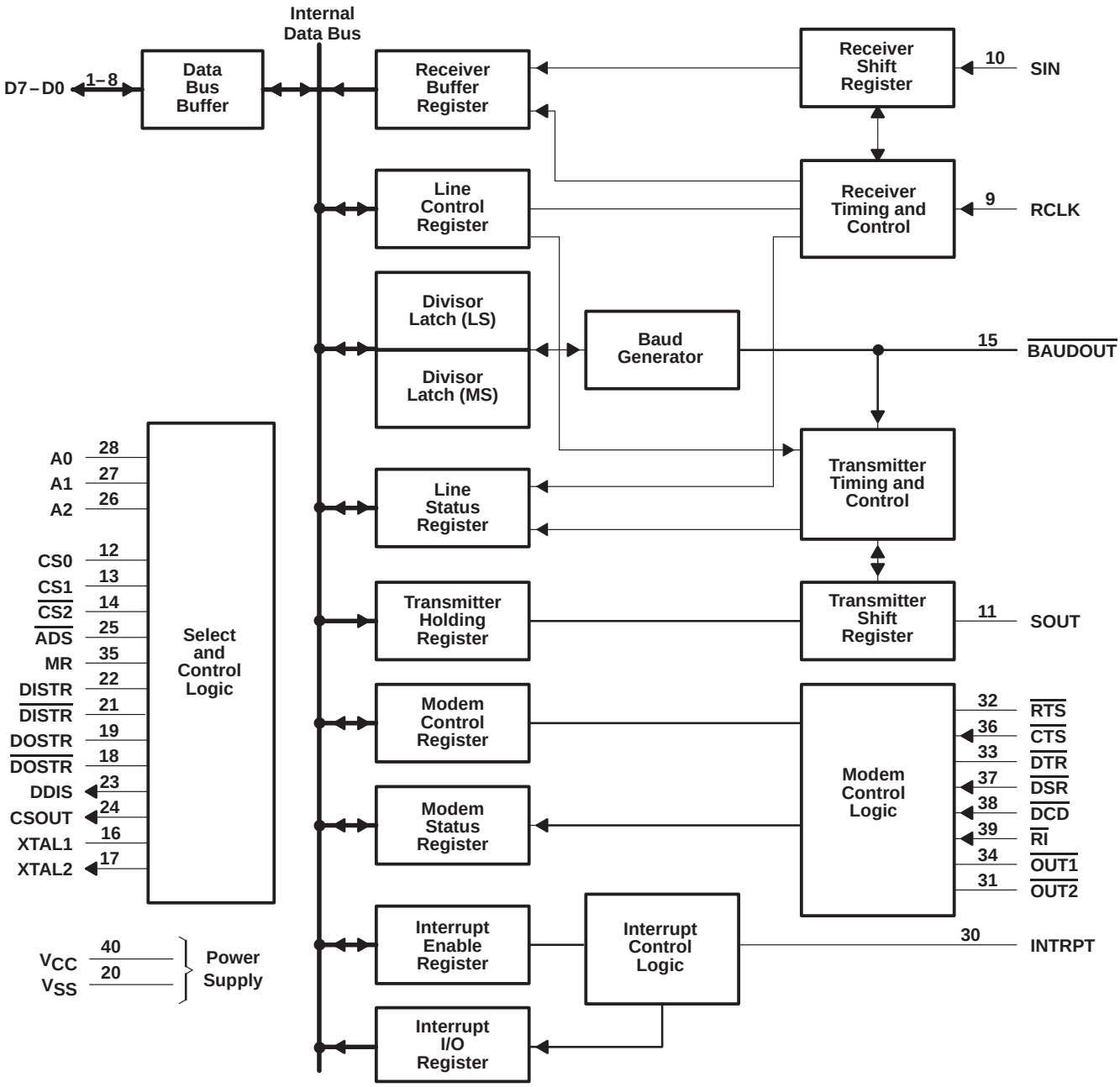
description (continued)

The TL16C450 performs serial-to-parallel conversion on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. The CPU can read and report on the status of the ACE at any point in the ACE's operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered.

The TL16C450 ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to ($2^{16} - 1$) and producing a 16× clock for driving the internal transmitter logic. Provisions are included to use this 16× clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

block diagram



Terminal numbers shown are for the N package.

Terminal Functions

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
A0 A1 A2	28 27 26	I	Register select. A0, A1, and A2 are three inputs used during read and write operations to select the ACE register to read from or write to. Refer to Table 1 for register addresses, also refer to the address strobe ($\overline{ADS}$) signal description.
$\overline{ADS}$	25	I	Address strobe. When $\overline{ADS}$ is active (low), the register select signals (A0, A1, and A2) and chip select signals (CS0, CS1, $\overline{CS2}$) drive the internal select logic directly; when high, the register select and chip select signals are held in the state they were in when the low-to-high transition of $\overline{ADS}$ occurred.
$\overline{BAUDOUT}$	15	O	Baud out. $\overline{BAUDOUT}$ is a16× clock signal for the transmitter section of the ACE. The clock rate is established by the reference oscillator frequency divided by a divisor specified by the baud generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
CS0 CS1 $\overline{CS2}$	12 13 14	I	Chip select. When CSx is active (high, high, and low respectively), the ACE is selected. Refer to the $\overline{ADS}$ signal description.
CSOUT	24	O	Chip select out. When CSOUT is high, it indicates that the ACE has been selected by the chip select inputs (CS0, CS1, and $\overline{CS2}$). CSOUT is low when the chip is deselected.
$\overline{CTS}$	36	I	Clear to send. $\overline{CTS}$ is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when $\overline{CTS}$ changes state, an interrupt is generated.
D0 – D7	1 – 8	I/O	Data bus. D0 – D7 are 3-state data lines that provide a bidirectional path for data, control, and status information between the ACE and the CPU.
$\overline{DCD}$	38	I	Data carrier detect. $\overline{DCD}$ is a modem status signal. Its condition can be checked by reading bit 7 (DCD) of the modem status register. Bit 3 (DDCD) of the modem status register indicates that this signal has changed states since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DCD}$ changes state, an interrupt is generated.
DDIS	23	O	Driver disable. DDIS is active (high) when the CPU is not reading data. When active, this output can disable an external transceiver.
DISTR $\overline{DISTR}$	22 21	I	Data input strobes. When either DISTR or $\overline{DISTR}$ is active (high or low respectively) while the ACE is selected, the CPU is allowed to read status information or data from a selected ACE register. Only one of these inputs is required for the transfer of data during a read operation. The other input should be tied in its inactive state (i.e., DISTR tied low or $\overline{DISTR}$ tied high).
DOSTR $\overline{DOSTR}$	19 18	I	Data output strobes. When either DOSTR or $\overline{DOSTR}$ is active (high or low respectively), while the ACE is selected, the CPU is allowed to write control words or data into a selected ACE register. Only one of these inputs is required to transfer data during a write operation. The other input should be tied in its inactive state (i.e., DOSTR tied low or $\overline{DOSTR}$ tied high).
$\overline{DSR}$	37	I	Data set ready. $\overline{DSR}$ is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates that this signal has changed state since the last read from the modem status register. If the modem status interrupt is enabled when the $\overline{DSR}$ changes state, an interrupt is generated.
$\overline{DTR}$	33	O	Data terminal ready. When active (low), $\overline{DTR}$ informs a modem or data set that the ACE is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit of the modem control register to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a master reset or during loop mode operation or clearing bit 0 (DTR) of the modem control register.
INTRPT	30	O	Interrupt. When active (high), INTRPT informs the CPU that the ACE has an interrupt to be serviced. The four conditions that cause an interrupt are: a receiver error, received data is available, the transmitter holding register is empty, or an enabled modem status interrupt. The INTRPT output is reset (inactivated) either when the interrupt is serviced or as a result of a master reset.
MR	35	I	Master reset. When active (high), MR clears most ACE registers and sets the state of various output signals. Refer to Table 2 for ACE reset functions.

† Terminal numbers shown are for the N package.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.†	I/O	DESCRIPTION
$\overline{OUT1}$ $\overline{OUT2}$	34 31	O	Outputs 1 and 2. $\overline{OUT1}$ and $\overline{OUT2}$ are user-designated output terminals that are set to their active states by setting their respective modem control register bits (OUT1 and OUT2) high. $\overline{OUT1}$ and $\overline{OUT2}$ are set to their inactive (high) states as a result of master reset or during loop mode operations or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the MCR.
RCLK	9	I	Receiver clock. RCLK is the 16× baud rate clock for the receiver section of the ACE.
$\overline{RI}$	39	I	Ring indicator. $\overline{RI}$ is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that the $\overline{RI}$ input has transitioned from a low to a high state since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{RTS}$	32	O	Request to send. When active, $\overline{RTS}$ informs the modem or data set that the ACE is ready to transmit data. $\overline{RTS}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the MCR.
SIN	10	I	Serial input. SIN is the serial data input from a connected communications device.
SOUT	11	O	Serial output. SOUT is the composite serial data output to a connected communication device. SOUT is set to the marking (set) state as a result of MR.
V_{CC}	40		5-V supply voltage
V_{SS}	20		Supply common
XTAL1 XTAL2	16 17	I/O	External clock. XTAL1 and XTAL2 connect the ACE to the main timing reference (clock or crystal).

† Terminal numbers shown are for the N package.

absolute maximum ratings over free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range at any input, V_I . . . . . –0.5 V to 7 V
Output voltage range, V_O . . . . . –0.5 V to 7 V
Continuous total power dissipation at (or below) 70°C free-air temperature: FN package . . . . . 1100 mW
N package . . . . . 800 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	–0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}‡	HIgh-level output voltage	I_{OH} = –1 mA	2.4			V
V_{OL}‡	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
I_{Ikg}	Input leakage current	V_{CC} = 5.25 V, V_{SS} = 0, V_I = 0 to 5.25 V, All other terminals floating			±10	µA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V, V_{SS} = 0, V_O = 0 V to 5.25 V, Chip selected, write mode,or chip deselected			±20	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, T_A = 25°C, SIN, DSR, DCD, CTS, and RI at 2 V, All other inputs at 0.8 V, Baud rate = 50 kbits/s, XTAL1 at 4 MHz, No load on outputs			10	mA
C_{XTAL1}	Clock input capacitance	V_{CC} = 0, V_{SS} = 0, f = 1 MHz, T_A = 25°C, All other terminals grounded		15	20	pF
C_{XTAL2}	Clock output capacitance			20	30	pF
C_i	Input capacitance			6	10	pF
C_o	Output capacitance			10	20	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters apply for all outputs except XTAL2.

system timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	MIN	MAX	UNIT
t_{cR}	Cycle time, read ($t_{w7} + t_{d8} + t_{d9}$)		175		ns
t_{cW}	Cycle time, write ($t_{w6} + t_{d5} + t_{d6}$)		175		ns
t_{w5}	Pulse duration, $\overline{ADS}$ low	2,3	15		ns
t_{w6}	Pulse duration, write strobe	2	80		ns
t_{w7}	Pulse duration, read strobe	3	80		ns
t_{wMR}	Pulse duration, master reset		1000		ns
t_{su1}	Setup time, address valid before $\overline{ADS}\uparrow$	2,3	15		ns
t_{su2}	Setup time, CS valid before $\overline{ADS}\uparrow$	2,3	15		ns
t_{su3}	Setup time, data valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	2	15		ns
t_{h1}	Hold time, address low after $\overline{ADS}\uparrow$	2,3	0		ns
t_{h2}	Hold time, CS valid after $\overline{ADS}\uparrow$	2,3	0		ns
t_{h3}	Hold time, CS valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	2	20		ns
t_{h4}§	Hold time, address valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	2	20		ns
t_{h5}	Hold time, data valid after $\overline{WR1}\uparrow$ or WR2$\downarrow$	2	15		ns
t_{h6}	Hold time, CS valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	3	20		ns
t_{h7}§	Hold time, address valid after $\overline{RD1}\uparrow$ or RD2$\downarrow$	3	20		ns
t_{d4}§	Delay time, CS valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	2	15		ns
t_{d5}§	Delay time, address valid before $\overline{WR1}\downarrow$ or WR2$\uparrow$	2	15		ns
t_{d6}	Delay time, write cycle, $\overline{WR1}\uparrow$ or WR2$\downarrow$ to $\overline{ADS}\downarrow$	2	80		ns
t_{d7}§	Delay time, CS valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	3	15		ns
t_{d8}§	Delay time, address valid to $\overline{RD1}\downarrow$ or RD2$\uparrow$	3	15		ns
t_{d9}	Delay time, read cycle, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to $\overline{ADS}\downarrow$	3	80		ns

§ Only applies when ADS is low.

system switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w1}	Pulse duration, clock high	1	f = 9 MHz maximum	50		ns
t_{w2}	Pulse duration, clock low	1	f = 9 MHz maximum	50		ns
t_{d3}	Delay time, select to CS output	2,3†	C_L = 100 pF		70	ns
t_{d10}	Delay time, $\overline{RD1}\downarrow$ or RD2$\uparrow$ to data valid	3	C_L = 100 pF		60	ns
t_{d11}	Delay time, $\overline{RD1}\uparrow$ or RD2$\downarrow$ to floating data	3	C_L = 100 pF	0	60	ns
$t_{dis(R)}$	Disable time, $\overline{RD1}\downarrow\uparrow$ or RD2$\uparrow\downarrow$ to DDIS$\uparrow\downarrow$	3	C_L = 100 pF		60	ns

† Only applies when $\overline{ADS}$ is low.

baud generator switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{w3}	Pulse duration, $\overline{BAUDOUT}$ low	1	f = 6.25 MHz, CLK ÷ 1, C_L = 100 pF	80		ns
t_{w4}	Pulse duration, $\overline{BAUDOUT}$ high	1	f = 6.25 MHz, CLK ÷ 1, C_L = 100 pF	80		ns
t_{d1}	Delay time, XIN$\uparrow$ to $\overline{BAUDOUT}\uparrow$	1	C_L = 100 pF		125	ns
t_{d2}	Delay time, XIN$\uparrow\downarrow$ to $\overline{BAUDOUT}\downarrow$	1	C_L = 100 pF		125	ns

receiver switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d12}	Delay time, RCLK to sample clock	4			100	ns
t_{d13}	Delay time, stop to set RCV error interrupt or read RDR to LSI interrupt or stop to $\overline{RXRDY}\downarrow$	4		1	1	RCLK cycles
t_{d14}	Delay time, read RBR/LSR to reset interrupt	4	C_L = 100 pF		140	ns

transmitter switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d15}	Delay time, INTRPT to transmit start	5		8	24	baudout cycles
t_{d16}	Delay time, start to interrupt	5		8	8	baudout cycles
t_{d17}	Delay time, WR THR to reset interrupt	5	C_L = 100 pF		140	ns
t_{d18}	Delay time, initial write to interrupt (THRE)	5		16	32	baudout cycles
t_{d19}	Delay time, read IIR to reset interrupt (THRE)	5	C_L = 100 pF		140	ns

modem control switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{d20}	Delay time, WR MCR to output	6	C_L = 100 pF		100	ns
t_{d21}	Delay time, modem interrupt to set interrupt	6	C_L = 100 pF		170	ns
t_{d22}	Delay time, RD MSR to reset interrupt	6	C_L = 100 pF		140	ns

PARAMETER MEASUREMENT INFORMATION

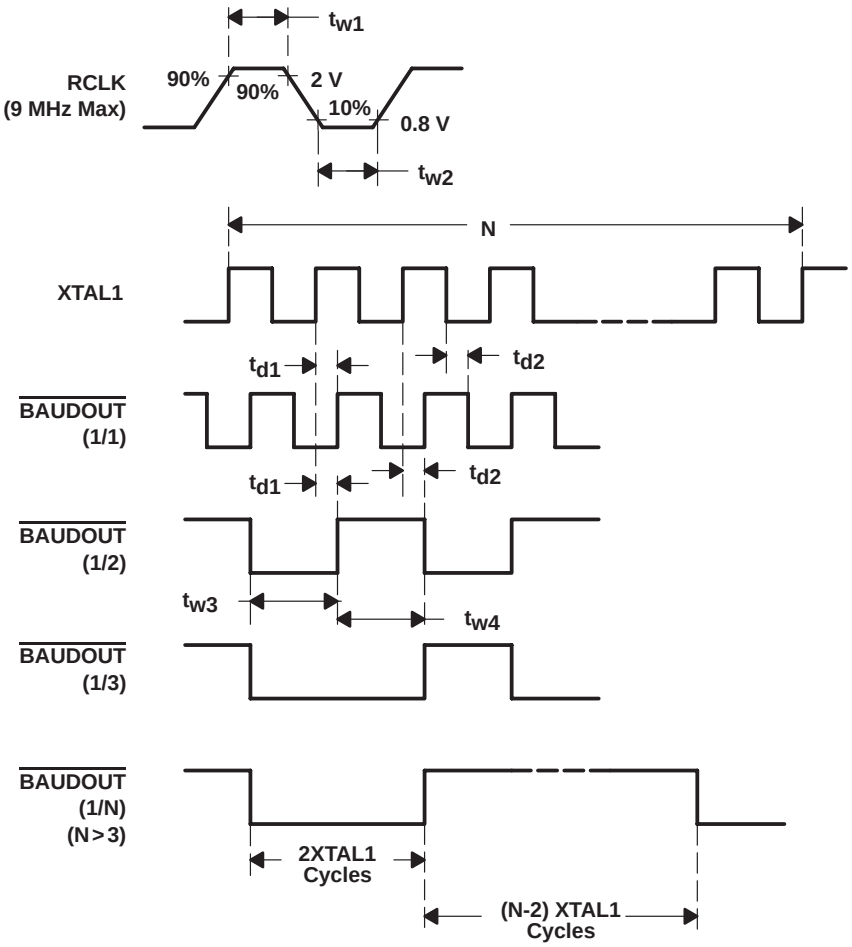
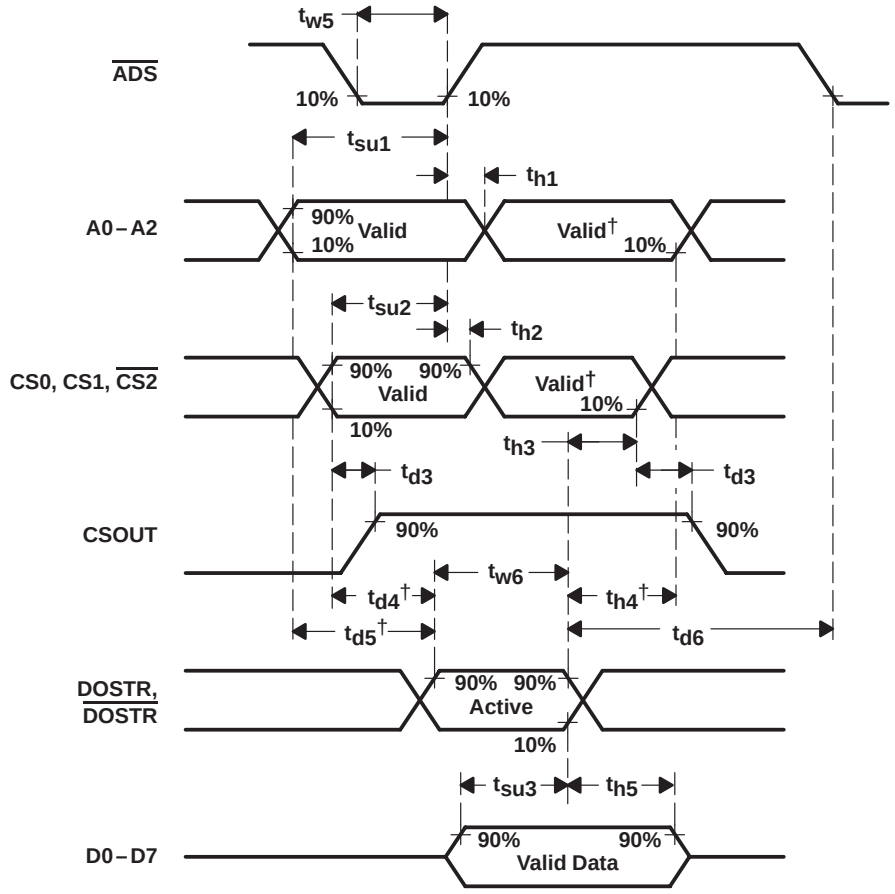


Figure 1. Baud Generator Timing Waveforms

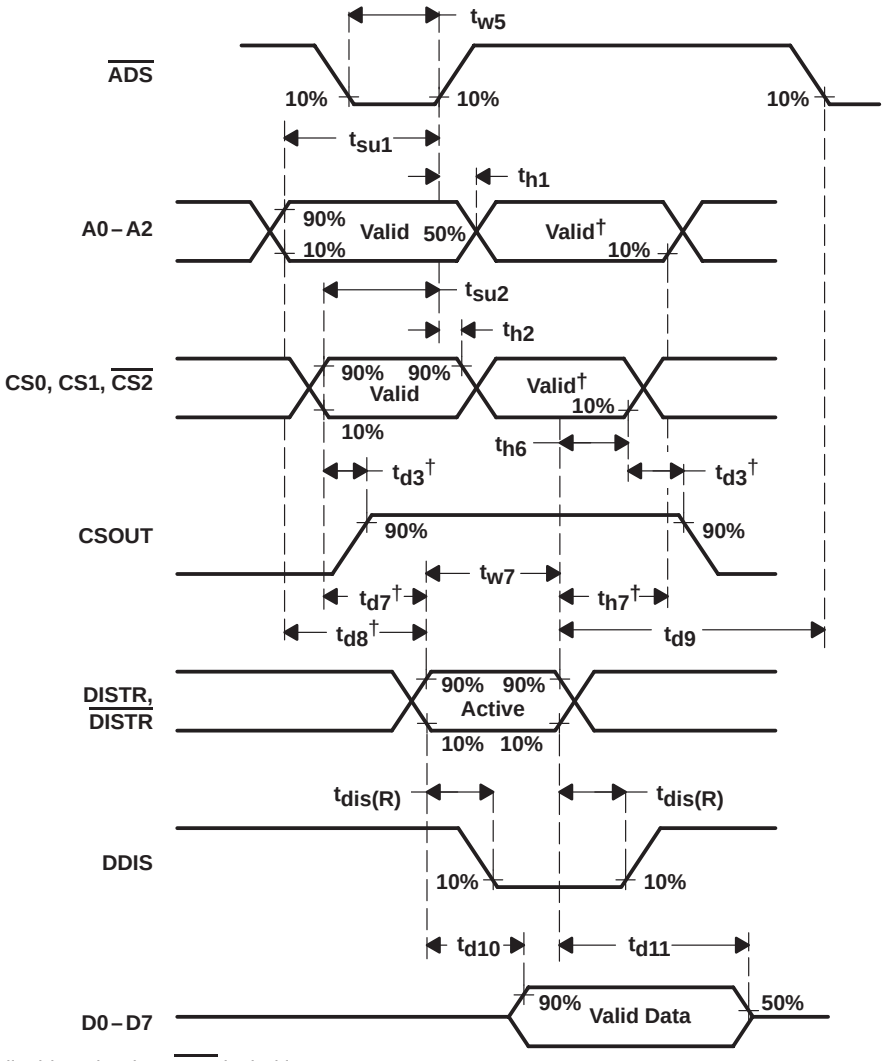
PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{\text{ADS}}$ is tied low.

Figure 2. Write Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



† Applicable only when $\overline{ADS}$ is tied low.

Figure 3. Read Cycle Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

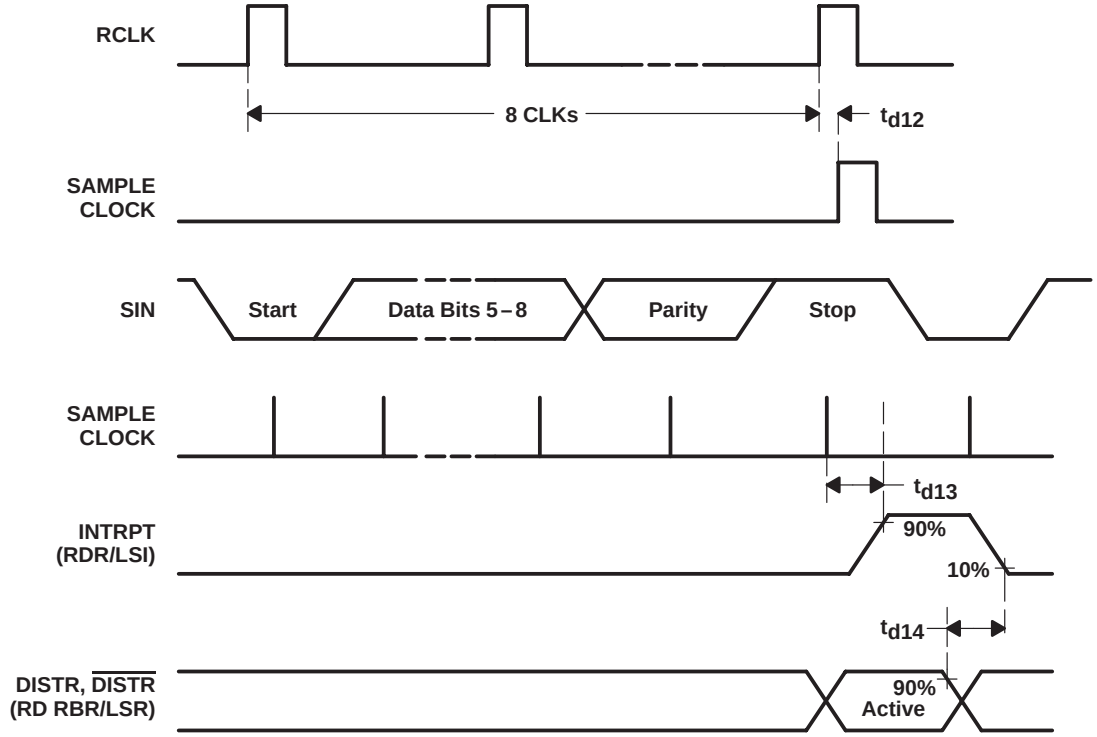


Figure 4. Receiver Timing Waveforms

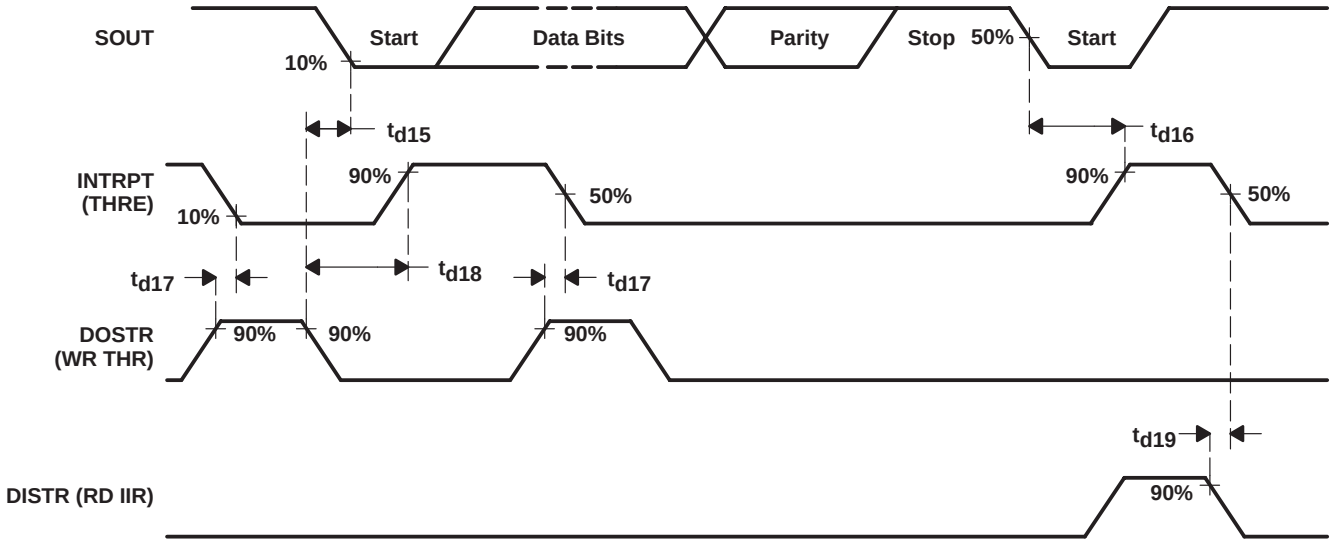


Figure 5. Transmitter Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

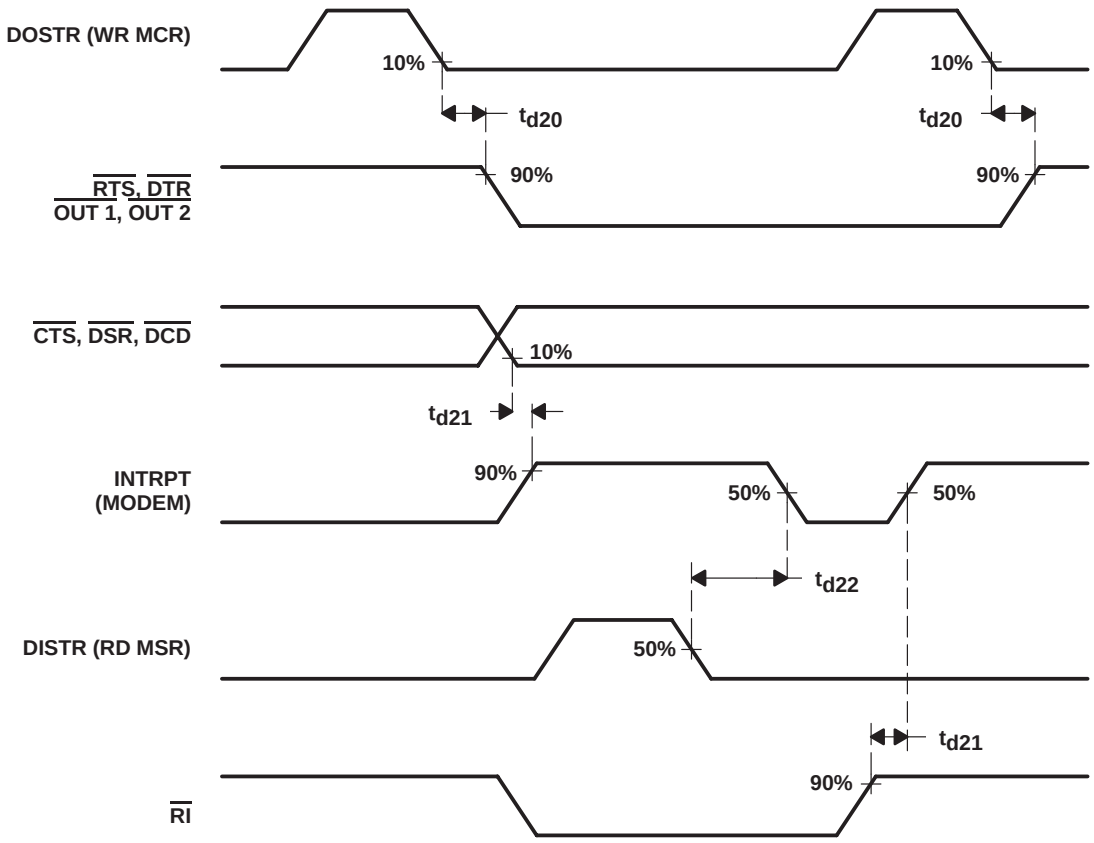


Figure 6. Modem Control Timing Waveforms

APPLICATION INFORMATION

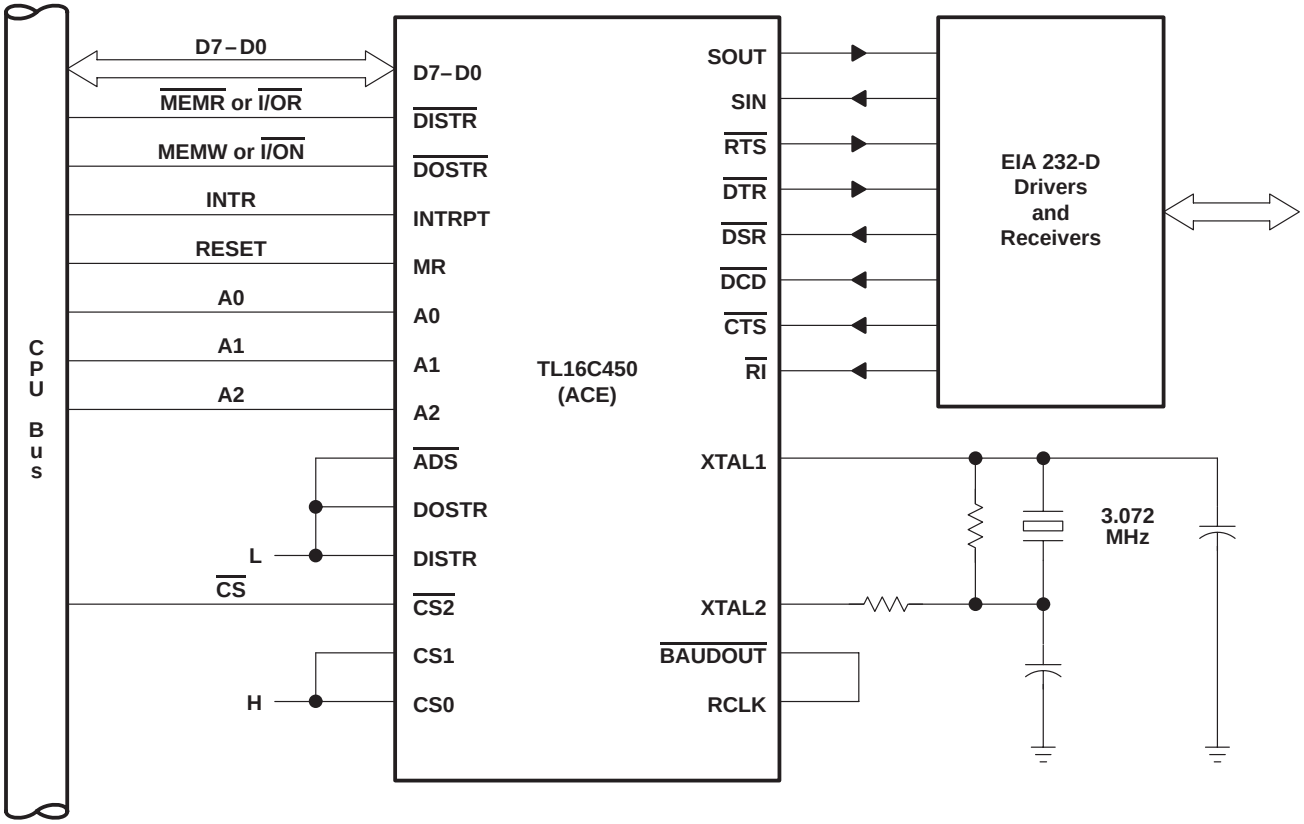


Figure 7. Basic TL16C450 Configuration

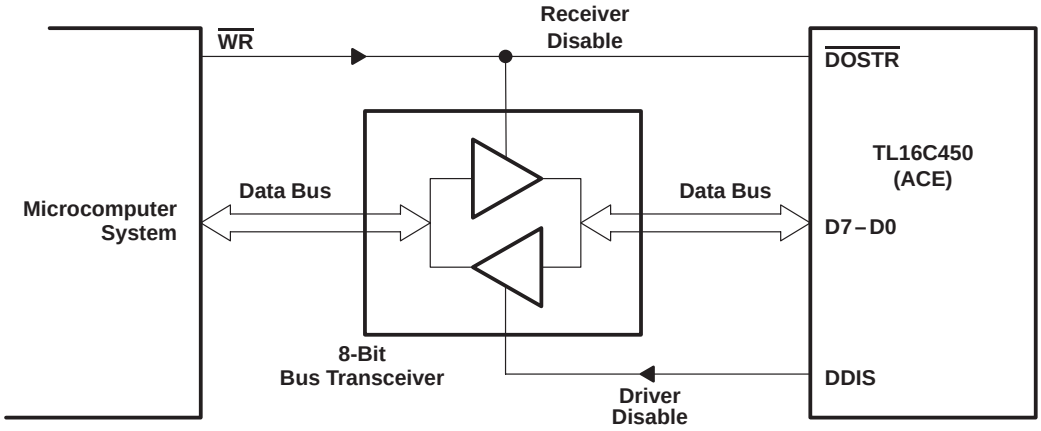


Figure 8. Typical Interface for a High-Capacity Data Bus

APPLICATION INFORMATION

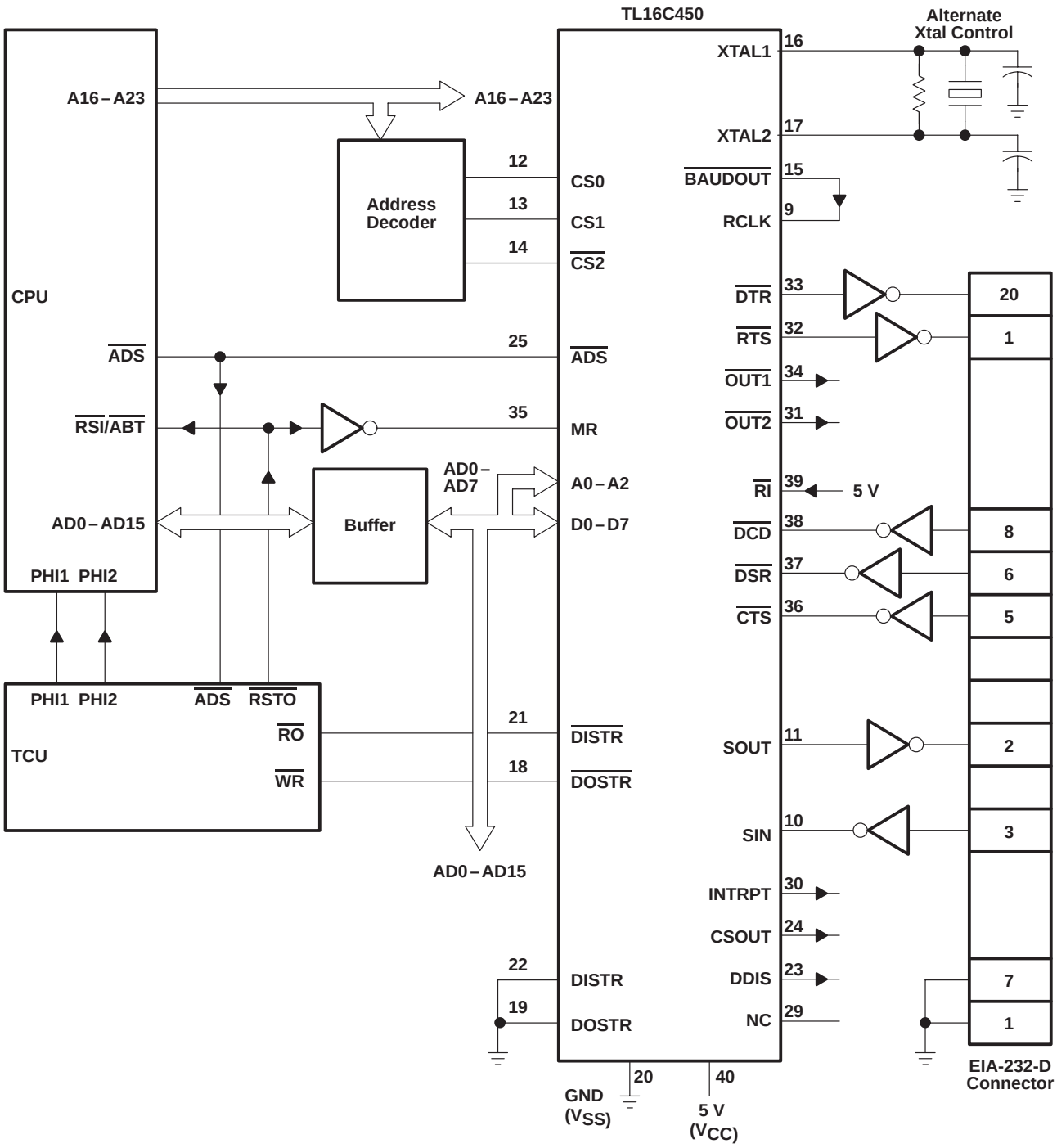


Figure 9. Typical TL16C450 Connection to a CPU

PRINCIPLES OF OPERATION

Table 1. Register Selection

DLAB†	A2	A1	A0	REGISTER
0	L	L	L	Receiver buffer (read), transmitter holding register (write)
0	L	L	H	Interrupt enable
X	L	H	L	Interrupt identification (read only)
X	L	H	H	Line control
X	H	L	L	Modem control
X	H	L	H	Line status
X	H	H	L	Modem status
X	H	H	H	Scratch
1	L	L	L	Divisor latch (LSB)
1	L	L	H	Divisor latch (MSB)

† The divisor latch access bit (DLAB) is the most significant bit of the line control register. The DLAB signal is controlled by writing to this bit location (see Table 3).

Table 2. ACE Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt enable register	Master reset	All bits low (0–3 forced and 4–7 permanent)
Interrupt identification register	Master reset	Bit 0 is high, bits 1 and 2 are low, and bits 3 –7 are permanently low
Line control register		All bits low
Modem control register	Master reset	All bits low
Line status register	Master reset	Bits 5 and 6 are high, all other bits are low
Modem status register	Master reset	Bits 0–3 are low, bits 4–7 are input signals
SOUT	Master reset	High
INTRPT (receiver error flag)	Read LSR/MR	Low
INTRPT (received data available)	Read RBR/MR	Low
INTRPT (transmitter holding register empty)	Read IIR/Write THR/MR	Low
INTRPT (modem status changes)	Read MSR/MR	Low
$\overline{\text{OUT2}}$	Master reset	High
$\overline{\text{RTS}}$	Master reset	High
$\overline{\text{DTR}}$	Master reset	High
$\overline{\text{OUT1}}$	Master reset	High
Scratch register	Master reset	No effect
Divisor latch (LSB and MSB) register	Master reset	No effect
Receiver buffer register	Master reset	No effect
Transmitter holding register	Master reset	No effect

PRINCIPLES OF OPERATION

accessible registers

The system programmer, using the CPU, has access to and control over any of the ACE registers that are summarized in Table 3. These registers control ACE operations, receive data, and transmit data. Descriptions of these registers follow Table 3.

Table 3. Summary of Accessible Registers

Bit No.	REGISTER ADDRESS										
	O DLAB = 0	O DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	O DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register IER	Interrupt Ident. Register (Read Only)	Line Control Register LCR	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LSB)	Latch (MSB)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBF)	"0" If Interrupt Pending	Word Length Select Bit 0 (WLSO)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBE)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

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interrupt enable register (IER)

The IER enables each of the four types of interrupts (refer to Table 4) and the INTRPT output signal in response to an interrupt generation. By clearing bits 0 – 3, the IER can also disable the interrupt system. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit, when set, enables the received data available interrupt.
- Bit 1: This bit, when set, enables the THRE interrupt.
- Bit 2: This bit, when set, enables the receiver line status interrupt.
- Bit 3: This bit, when set, enables the modem status interrupt.
- Bits 4 – 7: These bits in the IER are not used and are always cleared.

interrupt identification register (IIR)

The ACE has an on-chip interrupt generation and prioritization capability that permits a flexible interface with most microprocessors.

The ACE provides four prioritized levels of interrupts:

- Priority 1 – Receiver line status (highest priority)
- Priority 2 – Receiver data ready or receiver character time out
- Priority 3 – Transmitter holding register empty
- Priority 4 – Modem status (lowest priority)

When an interrupt is generated, the IIR indicates that an interrupt is pending and the type of interrupt in its three least significant bits (bits 0, 1, and 2). The contents of this register are summarized in Table 3 and described in Table 4.

- Bit 0: This bit can be used either in a hardwire prioritized or polled interrupt system. When bit 0 is cleared, an interrupt is pending. When bit 0 is set, no interrupt is pending.
- Bits 1 and 2: These two bits identify the highest priority interrupt pending as indicated in Table 4.
- Bits 3 – 7: These bits in the IIR are not used and are always clear.

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interrupt identification register (IIR) (continued)

Table 4. Interrupt Control Functions

INTERRUPT IDENTIFICATION REGISTER			PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
BIT 2	BIT 1	BIT 0				
0	0	1	None	None	None	–
1	1	0	1	Receiver line status	Overrun error, parity error, framing error or break interrupt	Reading the line status register
1	0	0	2	Received data available	Receiver data available	Reading the receiver buffer Buffer register
0	1	0	3	Transmitter holding register empty	Transmitter holding register empty	Reading the interrupt identification register (if source of interrupt) or writing into the transmitter holding register
0	0	0	4	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading the modem status register

line control register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the LCR. In addition, the programmer is able to retrieve, inspect, and modify the contents of the LCR; this eliminates the need for separate storage of the line characteristics in system memory. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. These bits are encoded as shown in Table 5.

Table 5. Serial Character Word Length

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

- Bit 2: This bit specifies either one, one and one-half, or two stop bits in each transmitted character. When bit 2 is cleared, one stop bit is generated in the data. When bit 2 is set, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver checks the first stop bit only, regardless of the number of stop bits selected. The number of stop bits generated, in relation to word length and bit 2, is shown in Table 6.

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line control register (LCR) (continued)

Table 6. Number of Stop Bits Generated

Bit 2	Word Length Selected by Bits 1 and 2	Number of Stop Bits Generated
0	Any word length	1
1	5 bits	1 1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

- Bit 3: This bit is the parity enable bit. When bit 3 is set, a parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, if bit 3 is set, parity is checked. When bit 3 is cleared, no parity is generated or checked.
- Bit 4: This bit is the even parity select bit. When parity is enabled (bit 3 is set) and bit 4 is set, even parity (an even number of logic 1s is in the data and parity bits) is selected. When parity is enabled (bit 3 is set) and bit 4 is clear, odd parity (an odd number of logic 1s) is selected.
- Bit 5: This is the stick parity bit. When bits 3, 4, and 5 are set, the parity bit is transmitted and checked as cleared. When bits 3 and 5 are set and bit 4 is cleared, the parity bit is transmitted and checked as set.
- Bit 6: This bit is the break control bit. Bit 6 is set to force a break condition, i.e, a condition where the serial output terminal (SOUT) is forced to the spacing (cleared) state. When bit 6 is cleared, the break condition is disabled. The break condition has no affect on the transmitter logic, it only affects the serial output.
- Bit 7: This bit is the divisor latch access bit (DLAB). Bit 7 must be set to access the divisor latches of the baud generator during a read or write. Bit 7 must be cleared during a read or write to access the receiver buffer, the THR, or the IER.

line status register (LSR)†

The LSR provides information to the CPU concerning the status of data transfers. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the data ready (DR) indicator for the receiver. Bit 0 is set whenever a complete incoming character has been received and transferred into the RBR and is cleared by reading the RBR.
- Bit 1‡: This bit is the overrun error (OE) indicator. When bit 1 is set, it indicates that before the character in the RBR was read, it was overwritten by the next character transferred into the register. The OE indicator is cleared every time the CPU reads the contents of the LSR.
- Bit 2‡: This bit is the parity error (PE) indicator. When bit 2 is set, it indicates that the parity of the received data character does not match the parity selected in the LCR (bit 4). The PE bit is cleared every time the CPU reads the contents of the LSR.
- Bit 3‡: This bit is the framing error (FE) indicator. When bit 3 is set, it indicates that the received character does not have a valid (set) stop bit. The FE bit is cleared every time the CPU reads the contents of the LSR.
- Bit4‡: This bit is the break interrupt (BI) indicator. When bit 4 is set, it indicates that the received data input was held clear for longer than a full-word transmission time. A full-word transmission time is defined as the total time of the start, data, parity, and stop bits. The BI bit is cleared every time the CPU reads the contents of the LSR.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.
‡ Bits 1 through 4 are the error conditions that produce a receiver line-status interrupt.

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line status register (LSR)† (continued)

- Bit 5: This bit is the THRE indicator. Bit 5 is set when the THR is empty, indicating that the ACE is ready to accept a new character. If the THRE interrupt is enabled when the THRE bit is set, then an interrupt is generated. THRE is set when the contents of the THR are transferred to the transmitted shift register. This bit is cleared concurrent with the loading of the THR by the CPU.
- Bit 6: This bit is the transmitter empty (TEMT) indicator. Bit 6 is set when the THR and the transmitter shift register are both empty. When either the THR or the transmitter shift register contains a data character, the TEMT bit is cleared.
- Bit 7: This bit is always clear.

modem control register (MCR)

The MCR is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit (DTR) controls the data terminal ready ($\overline{\text{DTR}}$) output. Setting bit 0 forces the $\overline{\text{DTR}}$ output to its active state (low). When bit 0 is clear, $\overline{\text{DTR}}$ goes high.
- Bit 1: This bit (RTS) controls the request to send ($\overline{\text{RTS}}$) output in a manner identical to bit 0's control over the $\overline{\text{DTR}}$ output.
- Bit 2: This bit (OUT1) controls the output 1 ($\overline{\text{OUT1}}$) signal, a user designated output signal, in a manner identical to bit 0's control over the $\overline{\text{DTR}}$ output.
- Bit 3: This bit (OUT2) controls the output 2 ($\overline{\text{OUT2}}$) signal, a user designated output signal, in a manner identical to bit 0's control over the $\overline{\text{DTR}}$ output.
- Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When bit 4 is set, the following occurs:

  1. The SOUT is asserted high.
  2. The SIN is disconnected.
  3. The output of the transmitter shift register is looped back into the RSR input.
  4. The four modem control inputs ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, and $\overline{\text{RI}}$) are disconnected.
  5. The four modem control outputs ($\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{OUT1}}$, and $\overline{\text{OUT2}}$) are internally connected to the four modem control inputs.
  6. The four modem control output terminals are forced to their inactive states (high).

  In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify the transmit and receive data paths to the ACE. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational but the modem control interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. All interrupts are still controlled by the IER.

- Bits 5 through 7: These bits are clear.

† The line status register is intended for read operations only; writing to this register is not recommended outside of a factory testing environment.

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modem status register (MSR)

The MSR is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provides change information; when a control input from the modem changes state the appropriate bit is set. All four bits are cleared when the CPU reads the MSR. The contents of this register are summarized in Table 3 and are described in the following bulleted list.

- Bit 0: This bit is the delta clear to send (DCTS) indicator. Bit 0 indicates that the $\overline{\text{CTS}}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 1: This bit is the delta data set ready (DDSR) indicator. Bit 1 indicates that the $\overline{\text{DSR}}$ input has changed states since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 2: This bit is the trailing edge of ring indicator (TERI) detector. Bit 2 indicates that the $\overline{\text{RI}}$ input to the chip has changed from a low to a high state. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 3: This bit is the delta data carrier detect (DDCD) indicator. Bit 3 indicates that the $\overline{\text{DCD}}$ input to the chip has changed state since the last time it was read by the CPU. When this bit is set and the modem status interrupt is enabled, a modem status interrupt is generated.
- Bit 4: This bit is the complement of the clear to send ($\overline{\text{CTS}}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCR bit 1 (RTS).
- Bit 5: This bit is the complement of the data set ready ($\overline{\text{DSR}}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCR bit 0 (DTR).
- Bit 6: This bit is the complement of the ring indicator ($\overline{\text{RI}}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCRs bit 2 (OUT1).
- Bit 7: This bit is the complement of the data carrier detect ($\overline{\text{DCD}}$) input. When bit 4 (loop) of the MCR is set, this bit is equivalent to the MCRs bit 3 (OUT2).

programmable baud generator

The ACE contains a programmable baud generator that takes a clock input in the range between dc and 9 MHz and divides it by a divisor in the range between 1 and ($2^{16} – 1$). The output frequency of the baud generator is sixteen times (16×) the baud rate. The formula for the divisor is:

$$\text{divisor \#} = \text{XTAL1 frequency input} \div (\text{desired baud rate} \times 16)$$

Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the ACE in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

Tables 7 and 8 illustrate the use of the baud generator with crystal frequencies of 1.8432 MHz and 3.072 MHz, respectively. For baud rates of 38.4 kilobits per second and below, the error obtained is very small. The accuracy of the selected baud rate is dependent on the selected crystal frequency.

Refer to Figure 10 for examples of typical clock circuits.

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Table 7. Baud Rates Using a 1.8432-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 8. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

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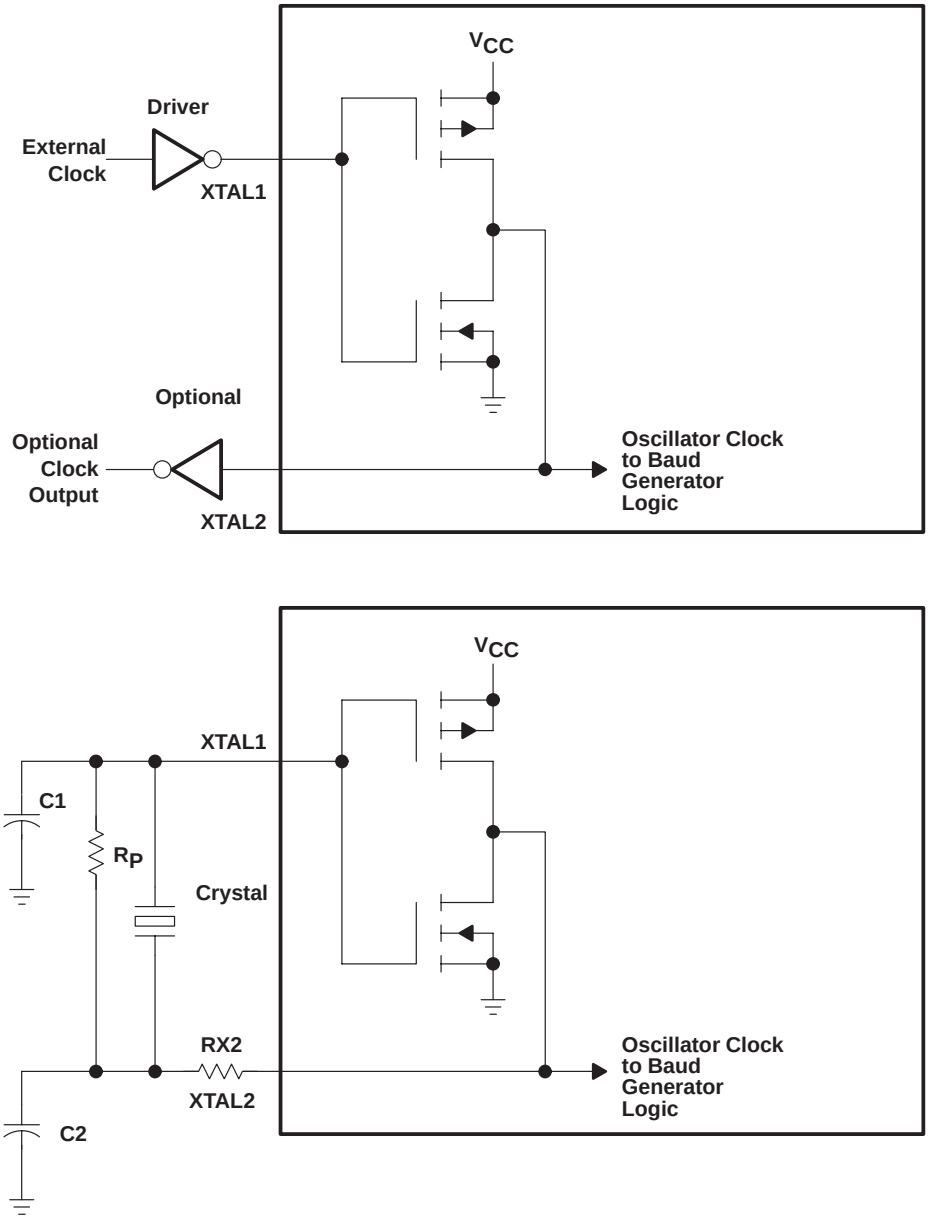

TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	R_P	RX2	C1	C2
3.1 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

Figure 10. Typical Clock Circuits

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receiver buffer register (RBR)

The ACE receiver section consists of a receiver shift register and a RBR. Timing is supplied by the 16× receiver clock (RCLK). Receiver section control is a function of the ACE line control register.

The ACE receiver shift register receives serial data from the serial input (SIN) terminal. The receiver shift register then converts the data to a parallel form and loads it into the RBR. When a character is placed in the RBR and the received data available interrupt is enabled, an interrupt is generated. This interrupt is cleared when the data is read out of the RBR.

scratch register

The scratch register is an 8-bit register that is intended for programmer use as a scratchpad, in the sense that it temporarily holds programmer data without affecting any other ACE operation.

transmitter holding register (THR)

The ACE transmitter section consists of a THR and a transmitter shift register. Timing is supplied by the baud out ($\overline{\text{BAUDOUT}}$) clock signal. Transmitter section control is a function of the ACE line control register.

The ACE THR receives data from the internal data bus and, when the shift register is idle, moves it into the transmitter shift register. The transmitter shift register serializes the data and outputs it at the serial output (SOUT). If the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled, an interrupt is generated. This interrupt is cleared when a character is loaded into the register.

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